REMARKS

After the foregoing amendment, claims 1-8 and 10-18 are active in the present application. Reconsideration and allowance of the application, as amended, are respectfully requested.

Claims 1-8 and 10-17 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Office Action states that it is unclear (in claims 1 and 10) what is meant by "the land area has at least one sharp edge that assists a pattern recognition system of a wire bonder in locating the at least one bond wire on the land area." And what materials make up or represent the photo mask area, and what are the sharp edges. Applicants respectfully traverse the rejection.

The present invention is directed to a bonding pad to which a bond wire is attached. The bonding pad includes, *inter alia*, a photo mask area; a clearance area; and a land area. Claim 1 recites that "at least one of the photo mask area, the clearance area, and the land area has at least one sharp edge that assists a pattern recognition system of a wire bonder in locating the at least one bond wire on the land area". A sharp edge refers to a well defined boundary of a bonding pad that facilitates a pattern recognition system of a wire bonder locating the bonding pad, which facilitates placement of the wire during the wire bonding process.

The problem being solved is that of accurately locating wires on bonding pads in view of the fact that the size of the pads has decreased (more pads per unit area).

In FIG. 3, the photo mask area 32 and the clearance area 34 are rectangular shaped, while the land area 36 is circular. The sides of the rectangular are "sharp edges," as opposed to the sides of the circular land area 36. That is, the circular land area 36 does not have sharp edges, but the photo mask area and the clearance area do have sharp edges. This configuration is supported in the specification at paragraph

[0024], which recites that, "In this embodiment, the photo mask area 32 and the clearance area 34 are rectangular".

As stated at paragraph [0022], the photo mask area 32 comprises a solder mask over BT (the substrate material).

In FIG. 4, the photo mask area 44, the land area 42 and the clearance area 46 are all rectangular and all have sharp edges, and the specification recites, "Thus, in this second embodiment, a photo mask area 44, a clearance area 46 and the land area 42 all have a plurality of sharp edges that assist the pattern recognition system ..." (Specification, para. [0024]).

In FIG. 6, the land area 70 includes cut-outs 67, such that there are many sharp edges that can be readily detected by the wire bonder pattern recognition system.

As discussed above, the photo mask area and the sharp edges are described in the specification and shown in the drawings, and thus the usage of such terms in the claims is clear and definite. Accordingly, Applicants respectfully request that the rejection of claims 1-8 and 10-17 under 35 U.S.C. §112, second paragraph, be withdrawn.

Claims 1, 3-8, 10 and 12-17 were rejected under 35 U.S.C. §103 as unpatentable over U.S. Patent Application No. 2003/0082848 (Ohuchida). Applicants respectfully traverse the rejection.

As discussed above, the present invention is directed to solving the problem of accurately locating wires on bonding pads in view of the fact that the size of the pads has decreased (more pads per unit area).

Ohuchida, like the present invention, pertains to an IC that is connected with bond wires to a substrate, wherein the substrate has vias that provide a conductive path from a first side of the substrate to a second side of the substrate. The first side of the substrate has bonding pads and the second side has solder balls, with the pads and the balls being connected by way of the vias.

In particular, Ohuchida is directed to a means for solving the problem of solder balls falling off of the substrate due to poor or weak connections between the solder balls and the vias. To overcome the solder ball fall off problem, Ohuchida teaches providing the via holes with at least one convex part. That is, instead of regular, cylindrical holes, the vias have a somewhat irregular shape. For example, FIG. 3A shows a via hole 112 that has a circular inner surface 302 and an internal channel 304. The channel 304 allows gases generated during reflow to escape from the via.

The Office Action refers to FIGS. 1-12 generally and FIGS. 4G and 7A in particular. FIGS. 4A-4G illustrate steps in forming a semiconductor package. In FIG. 4A, a substrate 102 is provided and vias 112 (with internal channels 304) are formed in the substrate. In FIG. 4B, a conductive pattern is formed on one surface of the substrate. The conductive pattern includes land areas 120. In FIG. 4C, a solder mask is formed over the conductive pattern of the substrate. In FIG. 4D die attach paste is applied to the substrate and in FIG. 4E, a die is affixed to the substrate. In FIG. 4F, the die 100 is electrically connected to the substrate 102. More particularly, wires 110 are bonded to chip bonding pads 116 and the land areas 120. In addition, a mold compound is used to seal the chip and bond wires. Finally, in FIG. 4G, solder balls 108 are attached in the via holes 112. FIGS. 5A-5C further illustrate the solder ball attach process.

As regards FIGS. 4A-4G, the present invention is concerned with the wire bonding step carried out in FIG. 4F and in particular attaching wires 110 to the land areas 120.

As discussed above, claim 1 of the present invention is directed to a bonding pad including a photo mask area; a clearance area; and a land area, wherein at least one of the photo mask area, the clearance area, and the land area has at least one sharp edge that assists a pattern recognition system of a wire bonder in locating the at least one bond wire on the

land area. Looking at FIG. 4D, which best illustrates the land area 120 prior to wire bonding (which is comparable to the bonding pad of the present invention), it can be seen that the land area 120 includes neither a photo mask area nor a clearance area.

FIGS. 7A-7B, 8A-8C, 9A-9B and 10A of Ohuchida all show bottom views of various via holes, and do not show land areas that include either a photo mask area or a clearance area, as taught by the present invention.

In view of the foregoing discussion, Applicants submit that Ohuchida does not teach, suggest or disclose bonding pads that have either a photo mask area or a clearance area, as required by the claims of the present invention. Accordingly, Applicants respectfully request that the rejection of claims 1, 3-8, 10 and 12-17 under 35 U.S.C. §103 be withdrawn.

Claims 1-8 and 10-17 were rejected under 35 U.S.C. §103 as unpatentable over U.S. Patent No. 5,612,576 (Wilson). Applicants respectfully traverse the rejection.

Wilson is directed to a semiconductor packaged device that has a vent hole 16 located beneath the integrated circuit 22 in order to prevent delamination due to high high levels of moisture inside the package. FIGS. 2-3 of Wilson show a vent hole 16 surrounded by sealing cap 20 that covers a portion of an annular metal land 21. The land 21 is not used for receiving a wire and so the land 21 is not akin to the bonding pad of the present invention. As previously discussed, the present invention provides an improved bonding pad that assists pattern recognition software in a wire bonding machine in attaching a bond wire to the bond pad. Wilson does not teach, suggest or disclose such a bond pad or any of its claimed features.

Applicants submit that Wilson does not teach, suggest or disclose bonding pads that have either a photo mask area or a clearance area, as required by the claims of the present invention. Accordingly, Applicants respectfully request that

the rejection of claims 1-8 and 10-17 under 35 U.S.C. §103 be withdrawn.

In view of the foregoing amendment and remarks, claims 1-8 and 10-17, are now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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(Date)

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